ABSTRACT

A buffer delay control mechanism controls the operation of a packet buffer of a digitized packet-based transmission network. The packet buffer receives packets from the network and controllably reads out packets for application to a digitized packet signal processor. A nominal buffer delay is maintained in the absence of an increase in delay in receipt of packets from the network. In response to an increase in network delay, the buffer delay is increased, and thereafter maintained at the increased value in the absence of a further increase in delay in receipt of packets from the network. For any further increase in throughput delay, the buffer delay is again updated, so as to maintain the value of buffer delay at a value associated with maximum encountered transport delay through the network.